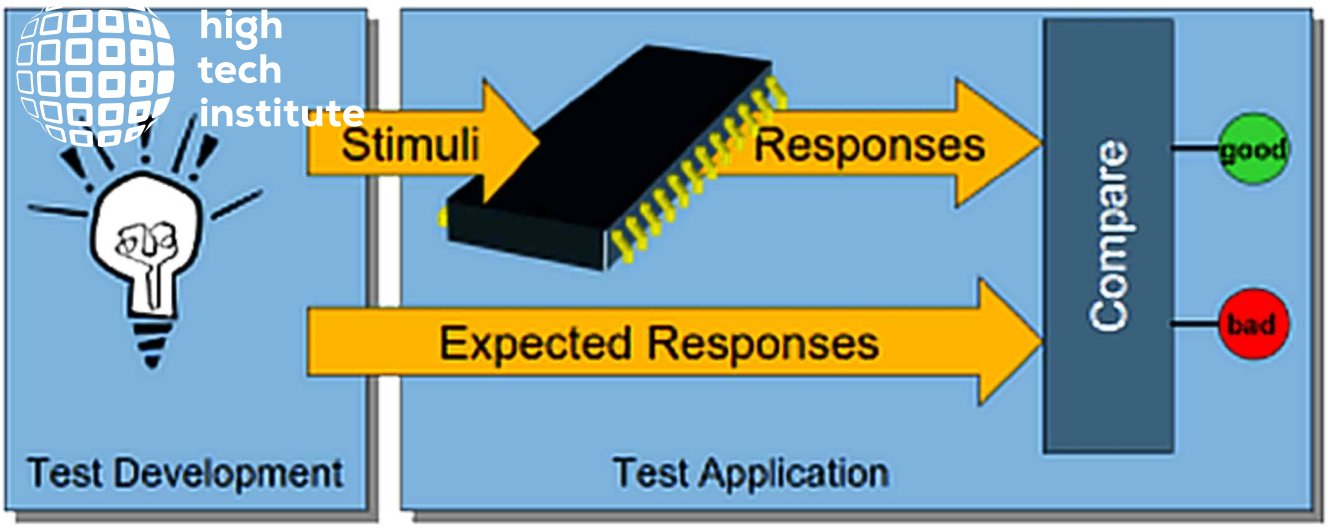
TRAINING BROCHURE

Test and design-for-test for digital integrated circuits training



Provisional reservation

Book now

high tech institute

Test and design-for-test for digital integrated circuits

Price: € 2,500 excl. VAT *

Duration: 4 consecutive days

Contact: training@hightechinstitute.nl, +31 85 401 3600

Score: 8.4 ★★★★☆

Intro

Integrated circuits (ICs) are integral part of any electronics system we see around. While the continue scaling of transistor feature sizes has been enhancing the chip density, the complexity of new generations of VLSI chips have been increasing; we already reached the point where billions of transistors are integrated on a single chip. Developing, designing and manufacturing of such chips are not only very complicated and time consuming, but also prone to defects; these may due to several deficiencies in the original silicon and in the manufacturing process. To guarantee the customers satisfaction, semiconductor companies have to ensure the required product quality and reliability of the manufactured chips through *testing* (e.g., at wafer level and after packaging). Moreover, It has been shown that tackling problems associated with testing VLSI chips at earlier design stage levels significantly reduces the testing cost. Thus it is important for hardware designers to be exposed to concepts of VLSI testing which can help them design better products at lower cost. Hence, appropriate test development is of key importance not only to ensure the customer satisfaction, but also to optimize the test cost.

This course covers the fundamentals of IC test and Design-for-Test; it introduces the participant to the field of digital systems testing and associated aspects. The participant will learn that ensuring customer satisfaction needs appropriate countermeasures to be taken, both during the design phase (i.e., part of the design), but also after manufacturing, and even in field/ during the lifetime of the application (i.e., continue monitoring and acting when needed). The course will teach the participant how to guarantee that a chip that may consists of billions of transistors and connections can be tested in e.g., less than one second, how to ensure that the lifetime of the chip is 10 years rather than 2 years, etc. Topics that will covered include: importance of VLSI test, test process and Automatic Test Equipment (ATE), defects and fault modelling, Fault simulation, Testability Measurements, Combinational Circuit Testing, sequential Circuit Testing, Memory Testing, Design for Testability, Scan Design, Boundary Scan, Built-in-Self Test, Delay Test, Current Testing, IC reliability, etc.

The presenter of this course is a world-renowned speaker in the field with broad scientific and industrial experience. The speaker has presented his course material at many international conferences, as well at leading semiconductor companies (in Asia, USA, and Europe).

This training is available for open enrollment as well as for in-company sessions. For in-company sessions, the training can be adapted to your situation and special needs.

Certification

Participants will receive a High Tech Institute course certificate for attending this training.

Course leader

Hans Vink MSc

Trainers

Prof. Dr. Ir. S. Hamdioui

** Prices are subject to change. Price correction will be applied at the end of the year.*

Keep me posted

Objective

After the course, the participant will:

- understand the importance of VLSI testing and reliability, its impact on the total cost and the quality of the designed product;
- be aware about the different testing stages and types;
- have a good understanding of the functions of IC test equipment and its main components;
- be able to describe the silicon/ transistor/ interconnect defect mechanisms and their associated fault models, and how they can be tested;
- examine different test methodologies for logic/sequential circuits and (embedded) memories, their advantages, disadvantages, cost, limitations, etc.
- analyze different “Design-for-Testability DFT” methodologies, their advantages, disadvantages, cost and limitations
- develop test solutions for defined faults models for logic circuits, sequential circuits and (embedded) memories; and make a reasoned choice from available tests and Design-for-Test techniques;
- better understand the “weaknesses” of digital systems regarding test and reliability;
- become a better VLSI designer, a better test engineer/ product engineer;
- be able to follow other IC test courses and tool trainings more effectively.

Target audience

This course is intended for those involved in the design and/or testing of digital integrated circuits and memories: Digital/memory IC design engineers, test and product engineers, fab engineers, test engineers, starting DfT engineers. Also: test researchers, test methodology developers, test tool developers and their managers!

Required background knowledge:

- Educational level: technical college / university in Electrical engineering, Computer, engineering or mathematics;
- Basic of digital synchronous IC design and manufacturing;
- Recommended: Several years of industrial practice.

Program

- Introduction to IC Test and Reliability;
- Test Execution: VLSI Test Process and Test Equipment;
- Fault (and Defects) Modeling;
- Fault Simulation;
- Testability Measurements;
- Combinational Circuit Testing;
- Sequential Circuit Testing;
- Memory Testing;
- Design-for-Testability: Scan Design;
- Design-for-Testability: Built-in-Self Test;
- Design-for-Testability: Boundary Scan;
- Special/ Advanced tests;
- IC Reliability: defects, models and test approaches;
- Modular (Core-Based) SOC Testing;
- Future trends and challenges in IC Test and Reliability.

Methods

A balanced mixture between interactive lectures and small exercises. Course material: lecture notes.

Frequency

Once per year

Read the interview:

Remarks from participants:

- ‘The level of training was very good. Good explanation of DfT in general and specifically for digital IC's.’ > Robert Mossel , Nexperia
- ‘Very useful. Very practical-oriented. Gives an excellent background on test aspects and how-to during different IC development phases. Highly recommended.’ > Kasia Nowak , Nexperia
- "Good overview of all DfT aspects." > René Segaar – NXP Semiconductors
- "The best content for anyone unaware of the DfT (or) a perfect introduction course of DfT." > Leonardo Davinci Darwin – NXP Semiconductors
- "I’ve learned a lot about DfT testing and the latest techniques being used nowadays. I grew as a test engineer during this course, in knowledge." > Ragy Magdy – NXP Semiconductors