Training Signal integrity of a PCB workshop

This training starts on: Expected June 2020

Location:	Eindhoven
Price:	1.200,00 euro excl. VAT
Duration:	2.5 consecutive days
Contact:	training@hightechinstitute.nl, +31 85 401 3600

Overview

The "fast edges" of modern electronic devices cause a lot of signal integrity (SI) problems. It is more and more difficult to use components within their specifications. The SI problems result in unexpected behavior of the hardware, reset problems, download problems, latch-ups, software hang-ups caused by the hardware and, last but not least, very noisy boards not compliant to FCC (USA), CISPR (EU) or VCCI (Japan).

In this very practical course for electronic designers, board- and IC designers, the theory behind signal integrity is explained and illustrated, practical problems are modelled and simulated, solutions are discussed and simulated. During the hands-on sessions the course participants use software to analyze system parts with SI problems and the effect of measures.

The course concentrates on signal integrity on a printed circuit board (PCB) and around the interface between board and IC. It does not cover aspects as architectures for fast systems.

Intended for

This workshop is primarily meant for system architects, electronic designers as well as board- and IC-designers, especially designers of reference designs and evaluation boards.
At least BSc in electronics / electrical engineering and a working relation with EMC.

Objective

After the course, the participant will:

- be able to recognize signal integrity problems of modern fast electronic systems;
- be able to analyze the signal integrity of a PCB;
- know and be able to apply methods to improve the signal integrity of a PCB;
- know IC characteristics that may cause signal integrity problems at a PCB.

Programme

Signal integrity problems may arise at many levels: within an IC, at the package level, on a PCB, at the backplane of boards, at inter-system communication.

There are issues that hold at various levels. But practical reasons often cause different approaches at different levels. This course concentrates on signal integrity on the PCB and around the interface between IC and PCB and is therefore highly relevant both for a PCB designer and an IC designer. The examples applied during the course, however, stem from the PCB area.

There are problems on signal integrity (and power integrity) that manifest themselves on a PCB but that should have been resolved on an IC. In case an IC strongly radiates (EMC), there are additional costs at PCB-level such as with housing or a metal shield, possibly the required performance may even not be reached. To prevent these problems

Partner

Certification

Participants will receive a High Tech Institute course certificate for attending this training.

Course leader

Hans Vink MSc

Teacher

Jack Leijssen BSc

Timetable

01-01-2030 | 06:00

the PCB designer might choose a chip set from another supplier.

Furthermore, a relationship exists between the pinning of an IC and the number of layers of a PCB. For financial reasons there is a strong preference for e.g. a 4 layers above a 6 layers PCB (costs are rising sharply with the number of layers). However, this can make demands on the pinning. If these demands are not handled properly, a 6 layer PCB might be necessary because of SI reasons. An alternative is to select an IC from another supplier.

Lessons:
- Signal integrity: high speed signal propagation, reflection, ringing, transmission-lines, termination, balanced lines, edge control, cross-talk, stack-up, simulation of high speed nets;
- Power integrity: high speed power distribution, power planes topology, board stack-up, bypassing capacitors, embedded passives, PCB production and materials, power supply noise classes, power integrity simulation demo;
- IBIS modelling: creating IBIS models, modifying models, understanding the most important parameters of an IBIS model;
- EMC introduction: EMC compliance tests, emission, immunity to RF fields, EFT, bursts, pre-compliance testing, ESD, latch-up;
- EMC signals: identify the sources of radiation, narrow spectra signals versus wide spectra signals, clamping noise, board stack-up improvements for EMC, crosstalk;
- EMC coupling and cabling: ground bounce, VCC coupling, optimisation of cable connections to a board, antenna's, radiation gain caused by cavities;
- EMC advanced partitioning: noise sources, SNR, common mode radiation versus differential mode, common mode isolation, unshielded housing, aperture antennas, creating common mode quite islands (moats);
- Cost-price optimisation: 2-layer boards for high speed, 4 layer boards, board production costs;
- High speed memory connection: DDRx and SSTL.

Hands-on sessions:
- Transmission line termination simulations, simulation of different board stack-ups;
- IBIS modelling, IBIS modelling theory, debugging IBIS models + IBIS editor;
- Topology simulation, board partitioning, crosstalk.

Methods

Lectures, PC exercises. Course material: course notes.